UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/770,890	02/02/2004	James M. Derderian	2269-4817.3US (01-0103.03	1094

24247 7590 06/07/2005

TRASK BRITT
P.O. BOX 2550
SALT LAKE CITY, UT 84110

EXAMINER	
THAI, LUAN C	

ART UNIT	PAPER NUMBER
2891	

DATE MAILED: 06/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/770,890	DERDERIAN, JAMES M.	
	Examiner	Art Unit	
	Luan Thai	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 3/31/05.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-33 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-33 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office action is responsive to the amendment filed March 31, 2005.

Claims 1-33 are pending in this application.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4, 11, 13-14, 16-18, 20-22, 24-25 and 31-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fogal et al (5,323,060 of record).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 1-4, 11, 16-18, 20-22, and 24-25, Fogal et al teach (see specifically figures 1-6, Col. 2-4) a method forming an assembly including semiconductor devices in stacked arrangement, comprising: providing a substrate (12) including a plurality of contact areas (from which bonding wires (44-50-56) are electrical connected); providing a first semiconductor device (18) on the substrate (12); placing bonding wires (44-50-56) between bond pads (26, see figure 2) on an active surface of the first semiconductor device (18) and corresponding contact area of the substrate (12), wherein the bonding wires (44-50-56) comprises discrete conductive elements (e.g., the

portions of bonding wires connected to the bond pad 26 of the semiconductor device) extending partially over the active surface of the first semiconductor device (18), applying an adhesive layer (38) at least to the active surface of the first semiconductor device (18), wherein the adhesive layer (38) has a thickness (40) (e.g., being 0.008 inch, Col.3, lines 3-4); placing a second semiconductor device (28) on the first semiconductor device (18), such that the active surface of the first semiconductor device (18) is space apart from a back side of a second semiconductor device (28) by the thickness (40) of the adhesive layer (38), and substantially curing the adhesive layer (38). Fogal et al further disclose that "*the adhesive layer 38 has a thickness 40 and is deposited to define an adhesive perimeter 42, with perimeter 42 being positioned within central area 24 inside of the peripheral bonding pads 26*" (Col. 2, lines 51-54). Since the thickness (or the height) and the perimeter (and thus the area) of the adhesive layer (38), which is positioned between the first and second devices, have been defined, the volume of the adhesive layer (38) is obvious to be determined, and that reads on the claimed of "*applying substantially a predetermined volume of adhesive material onto at least a surface of [a] first semiconductor device ...,*".

Regarding claims 13-14 and 31-32, although Fogal et al. do not explicitly teach a curing step for the adhesive material applied between the first and second devices, Fogal et al. do disclose the adhesive to be *a thermoplastic material* is disclosed (Col. 2, lines 67-68) and a curing step would be obviously present for such material to function as it intended. Thus, during the process of curing the *thermoplastic material*, a semisolid state must exist before the final solid state of that *thermoplastic material.*

3. Claims 1-4, 11, 13-18, 20-25 and 31-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al (6,388,313 of record) in view of Ogawa et al (4,388,128 of record).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 1-4, 11, 16-18, and 20-25, Lee et al disclose (see specifically figures 1-2) semiconductor devices in stacked arrangement and method of fabricating the same, comprising: providing a substrate (20) having plurality of external connection elements (27) on the bottom surface and a plurality of contact areas on the top surface (from which bonding wires (22/25) are electrical connected; mounting a first semiconductor device (21) on the substrate (20) via adhesive (28); electrical connecting bonding wires (22/25) between bond pads (210) on an active surface of the first semiconductor device (21) and corresponding contact areas on the substrate (20), wherein the bonding wires (22/25) comprises discrete conductive elements (e.g., the topmost bent portions of bonding wires 22 connected to the bond pad 210 of the first semiconductor device 21) extending partially over the active surface of the first semiconductor device (21), applying an amount of adhesive material (23) over the active surface of the first semiconductor device (21), wherein the adhesive layer (38) has a thickness enough to encapsulate the part of the bonding wires (22) that is positioned between the first semiconductor device (21) and a second semiconductor device (24), which is placed on the first device (21) thereafter (Col. 5, lines 41-45), and to space apart the active surface of the first semiconductor device (21) from a back side of the second semiconductor device (24); and encapsulating at least portions of the first device (21), the second device

(24), and the substrate (20) by a encapsulant (26). Lee et al. do not explicitly teach that the amount of adhesive material (23) is *"predetermined"*.

However, predetermining an amount of a material to be used in an assembly or a multi-chip module is a routine in a process of making. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to predetermine the volume of adhesive to be used in Lee et al's method since such predetermination is just a routine in the process of forming an assembly or a multi-chip module. Furthermore, Ogawa et al. while related to a similar bonding chip-to-chip design teaches: applying *a predetermined amount of adhesive* (124) to a surface of a first semiconductor device (120) and mounting a second semiconductor device (122) on the first device via the *predetermined amount of adhesive (124), and curing the adhesive* (Col. 9, lines 64-68 and Col. 10, lines 1-3). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Ogawa et al's teaching with Lee's method would have been beneficial because predetermining the amount of each of materials used in a product would help the product to be manufactured in mass production.

Regarding claims 13-14 and 31-32, the proposed method of Lee et al. and Ogawa, as assumed, teaches the adhesive being in liquid state and being cured (to form solid state) (see Ogawa's Col. 10, lines 1-9), a semisolid state of such thermosetting material inherently exist before the final solid state appeared at the end of the curing process.

Regarding claims 15 and 33, the proposed method of Lee et al. and Ogawa, as assumed, teaches a predetermined amount of adhesive being applied between a first

semiconductor device and a second semiconductor device, as detailed above. Since the adhesive is in liquid state and is cured (to form solid state), it would have been obvious to one of ordinary skill in the art at the time the invention was made to recognize that the distance (or the gap) between the first and second devices filled with the adhesive would be decreased as the adhesive being cured to change from liquid state to solid state.

4. Claims 5-10, 19 and 26-30, are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al (6,388,313 of record) and Ogawa et al (4,388,128), as applied to claims 1-4, 11, 13-18, 20-25 and 31-33 above, and further in view of Fujisawa et al (5,801,439 of record).

Regarding claims 5-10, 19 and 26-30, the proposed method of Lee et al and Ogawa et al teaches the claimed invention as detailed above except for the predetermined amount of adhesive *being introduced* between the first semiconductor device and the second semiconductor device.

Fujisawa et al while related to a similar method of forming semiconductor device in stacked arrangement teach, among the others, a step of inserting an adhesive (101) between two adjacent semiconductor devices (81c-81b-81a) (after mounting the upper device on the lower device) to support the upper side semiconductor device against the lower side semiconductor device (see Fig. 18, Col. 20, lines 59+, Col. 21, lines 1-3). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that modify the proposed method of Lee et al and Ogawa et al by positioning the second device on the first device and then inserting the predetermined amount of adhesive between two stacked devices, as taught by Fujisawa et al, would help to control the amount of adhesive used in the bonding process between two devices.

5. Claims 1-4, 11, 13-18, 20-25 and 31-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin (6,333,562 of record) in view of Ogawa et al (4,388,128).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 1-4, 11, 16-18, and 20-25, Lin teaches (see specifically figures 3-10, Col. 4-6) a method forming an assembly including semiconductor devices in stacked arrangement, comprising the steps: providing a substrate (e.g., a circuit board) (330) including a plurality of contact areas (330a); providing a first semiconductor device (310), which has a plurality of bonding pads (310a) formed on the active surface thereof, on the substrate (330) (Fig. 5); placing discrete conductive elements (e.g., bonding wires) (360) between bond pads 350a of the first semiconductor device (310) and corresponding contact areas (330a) of the substrate (330) to electrically connect the bond pads to the corresponding contact areas, wherein the discrete conductive elements (350b) extend partially over an active surface of the first semiconductor device (310) (Fig. 6). Lin further discloses the process steps: applying a volume of adhesive material (340) to the active surface of the first semiconductor device (310) before positioning the back side of a second semiconductor device (320) over the adhesive material (340) on the first semiconductor device (310). Since the second semiconductor device (320) is placed into the adhesive material (340) until contacting the protruding portions (350b) formed on the active surface of the first semiconductor device (Col. 5, lines 40-53), the distance between the active surface of the first semiconductor device (310) and the back side of the second semiconductor device (320) is decreased from substantially a set distance to

substantially a predetermined distance. Lin also discloses the steps of substantially curing the adhesive material (Col. 5, lines 54-62) and encapsulating at least portions of the first and second semiconductor devices, the discrete conductive elements (360-370) and the circuit board substrate (330) (see Col. 4, lines 39+). Lin does not explicitly teach the volume of adhesive material being *predetermined.*

However, predetermining an amount of a material to be used in an assembly or a multi-chip module is a routine in a process of making. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to predetermine the volume of adhesive to be used in Lin's method since such predetermination is just a routine in the process of forming an assembly or a multi-chip module. Furthermore, Ogawa et al. while related to a similar bonding chip-to-chip design teaches: applying *a predetermined amount of adhesive* (124) to a surface of a first semiconductor device (120) and mounting a second semiconductor device (122) on the first device via the *predetermined amount of adhesive (124), and curing the adhesive* (Col. 9, lines 64-68 and Col. 10, lines 1-3). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Ogawa et al's teaching with Lin's method would have been beneficial because predetermining the amount of each of materials used in a product would help the product to be manufactured in mass production.

Regarding claims 13-14 and 31-32, the proposed method of Lin and Ogawa, as assumed, teaches the adhesive being made of thermosetting material and being cured, a

semisolid state of such thermosetting material inherently exist before the final solid state appeared at the end of the curing process.

Regarding claims 15 and 33, the proposed method of Lin and Ogawa, as assumed, teaches a predetermined amount of adhesive being applied between a first semiconductor device and a second semiconductor device, as detailed above. Since the adhesive, as assumed in the proposed method of Lin and Ogawa, is in liquid state and is cured (to form solid state), it would have been obvious to one of ordinary skill in the art at the time the invention was made to recognize that the distance (or the gap) between the first and second devices filled with the adhesive would be decreased as the adhesive being cured to change from liquid state to solid state.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luan Thai whose telephone number is 571-272-1935. The examiner can normally be reached on 6:45 AM - 4:15 PM, Monday to Friday.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luan Thai whose telephone number is 571-272-1935. The examiner can normally be reached on 6:45 AM - 4:15 PM, Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nestor Ramirez can be reached on 571-272-2034. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Luan Thai
Primary Examiner
Art Unit 2891
June 2, 2005